WHAT IS CLAIMED IS:

1. A circuit, comprising:

a latch; and

a storage element coupled to the latch and, during programming of the storage element, the storage element avoids forwarding current from the storage element into the latch.

2. The circuit as recited in claim 1 is formed using a fabrication process capable of forming sub one-quarter micron features..

3. The circuit as recited in claim 1 is formed using a fabrication process that avoids additional steps or features needed to accommodate programming voltages that exceed twice the voltages on the latch.

4. The circuit as recited in claim 1, wherein the latch comprises a pair of cross-coupled inverters.

5. The circuit as recited in claim 4, further comprising a pair of pass-gate transistors coupled to a data bus to forward true and complementary bit values onto respective ones of the pair of cross-coupled inverters.

6. The circuit as recited in claim 1, further comprising a selecting transistor having a gate conductor and a source-to-drain path, and wherein the gate conductor is coupled through a programming transistor to an output of the latch, and the source-to-drain path is coupled between a ground supply and through a blocking transistor to the storage element.

7. The circuit as recited in claim 1, further comprising a blocking transistor having a source-to-drain path coupled between the storage element and through a programming transistor to an output of the latch

8. The circuit as recited in claim 1, wherein the storage element comprises a one-time programmable storage element.

9. The circuit as recited in claim 8, wherein the one-time programmable storage element comprises a dielectric that (i) upon receiving a programming voltage differential across the dielectric a relatively low resistive path will occur to a power supply, and (ii) upon receiving a non-programming voltage differential across the dielectric a relatively high resistive path will occur to the power supply.

10. A one-time programmable latching circuit, comprising:

a latch having two pairs of latching transistors connected to form a pair of cross-coupled inverters; and

a pair of one-time programmable storage elements coupled to respective outputs of the inverters, wherein the storage elements include a pair of storing transistors having a gate oxide thickness dissimilar from a gate oxide thickness of any of the set of latching transistors.

11. The latching circuit as recited in claim 10 is formed using a fabrication process capable of forming sub one-quarter micron features..

12. The latching circuit as recited in claim 10 is formed using a fabrication process that avoids additional steps or features needed to accommodate programming voltages that exceed twice the voltages on the latch.

13. The latching circuit as recited in claim 10, further comprising a data bus coupled to inputs of the pair of cross-coupled inverters.

14. The latching circuit as recited in claim 13, further comprising a selection circuit that includes a pair of programming transistors with source-to-drain paths coupled between inputs of the pair of cross-coupled transistors and gates of a pair of selecting transistors.

15. The latching circuit as recited in claim 14, wherein the programming transistors include a gate terminal adapted to receive a programming voltage and, upon receiving the programming voltage, one of the programming transistors causes programming current to flow from one of the pair of storage elements, through one of the pair of selecting transistors, and directly to a ground supply conductor configured within the latching circuit outside the latch.

16. The latching circuit as recited in claim 14, wherein the programming transistors include a gate terminal adapted to receive a programming voltage and, upon receiving the programming voltage, one of the programming transistors causes a binary value on the data bus to be placed on a gate of one of the pair of selecting transistors causing current to flow from one of the pair of storage elements, through one of the pair of selecting transistors, and directly to a ground supply conductor configured within the latching circuit outside the latch.

17. The latching circuit as recited in claim 10, wherein the latch further comprises a holding transistor coupled between each of the two pair of latching transistors to maintain a latched voltage value on the output of the pair of cross-coupled inverters during times when the holding transistor is activated.

18. The latching circuit as recited in claim 10, wherein the pair of one-time programmable storage elements further comprising a margin-testing transistor coupled to vary current from the pair of storage elements read as a voltage differential at an output of the pair of cross-coupled inverters.

19. The latching circuit as recited in claim 10, wherein the one-time programmable storage element comprises a dielectric that (i) upon receiving a programming voltage differential across the dielectric a relatively low resistive path will occur to a power supply, and (ii) upon receiving a non-programming voltage differential across the dielectric a relatively high resistive path will occur to the power supply.

20. A method for programming a programmable storage element, comprising:

latching a voltage value from a data bus onto an output of a pair of cross-coupled inverters;

forwarding the latched voltage value onto a gate of a selecting transistor to activate the selecting transistor; and

driving current from the programmable storage element through the activated selecting transistor to a ground supply conductor.

21. The method as recited in claim 20, wherein said forwarding comprises placing the voltage value that is greater than a threshold voltage above a ground supply onto the gate of the selecting transistor whose source terminal is coupled to the ground supply via the ground supply conductor.

22. The method as recited in claim 20, wherein said forwarding comprises placing the voltage value onto the gate of the selecting transistor during times when a source-to-drain path of a programming transistor is activated via a programming voltage placed on a gate of the programming transistor.

23. The method as recited in claim 20, wherein said driving comprises sending current across a gate oxide of a programmable transistor that forms the programmable storage element and through the source-to-drain path of the selecting transistor having a gate oxide dissimilar than the gate oxide of the programmable transistor.

24. The method as recited in claim 20, wherein said driving comprises sending current from the programmable storage element through a path outside the pair of cross-coupled inverters.

25. The method as recited in claim 20, wherein said latching comprises maintaining the voltage value onto the output of the pair of cross-coupled inverters after the voltage value from the data bus terminates.